EAST - [jig.wsp:1]

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Drafts
Pending
Active
L1: (183275) ROM or (read adj only adj memory)
L2: (4946) 1 and implant$3 and oxid$4
L3: (582) 2 and (oxid$4 near (substrate or sidewall$1))
L4: (337) 3 and buried
L5: (74) 4 and (thermal adj (oxidizing or oxide))
L6: (64) 5 and insulat$3
L7: (64) 6 and (conduct$3 or polysilicon)
L8: (46) 7 and (memory.clm. or ROM.clm. or (read adj2 memory).clm.)
L9: (37) 7 and (oxide.clm. or oxidizing.clm.)
L10: (37) 7 and (oxide.clm. or oxidizing.clm. or oxidation.clm. or oxidized.c
L11: (35) 10 and (oxid$4 near sidewall$1)
L12: (0) 10 and ((oxidizing or oxidation or oxidized) near sidewall$1)
Failed
Saved
(136) (substrate adj jig) or (jig adj substrate)
(99) ((substrate adj jig) or (jig adj substrate)) and (fix$3 or dicing or gri
(68) (((substrate adj jig) or (jig adj substrate)) and (fix$3 or dicing or gr
(28) ((((substrate adj jig) or (jig adj substrate)) and (fix$3 or dicing or g
(72) (((substrate adj jig) or (jig adj substrate)) and (flat$3 or warps$3)) a
(3960) jig.clm.
(495) jig.clm. and substrate
(35) (jig.clm. and substrate) and (((back adj grind) or dicing or (die adj bo
(0) (jig.clm. and substrate) and ((back adj grind) with jig)

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DBs | USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

7 and (oxide.clm. or oxidizing.clm. or oxidation.clm. or oxidized.clm.)

BRS form | ISR form | Image | Text | HTML

	V	L	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3	In
3			US 6509599 B1	20030121	26	Trench capacitor with insulation collar and method		257/304; 257/E21.651;		Forster, Kai et al.						US
4			US 6500768 B1	20021231	12	Method for selective removal of ONO layer	438/738	438/723; 438/724;		Shields, Jeffrey A. et al.						US
5			US 6433382 B1	20020813	27	Split-gate vertically oriented EEPROM device and p	257/315	257/329; 257/E29.129;		Otlowski, Marius et al.						US
6			US 6417040 B2	20020709	33	Method for forming memory array having a digit line bu	438/238	257/E21.648; 257/E27.089;		Noble, Wendell						US
7			US 6410391 B1	20020625	10	Method for producing an EEPROM memory cell with a tr	438/259	257/E21.645; 257/E21.653;		Gelsacher, Rudolf						US
8			US 6391707 B1	20020521	20	Method of fabricating nonvolatile memory device	438/257	257/E21.68; 257/E27.103;		Choi, Woong-Lim et al.						US
9			US 6200073 B1	20010313	31	Production method for a trench capacitor with an ins	438/386	257/E21.651; 438/242;		Schrems, Martin et al.						US
10			US 6191950 B1	20010220	11	Dense SOI programmable logic array structure	438/164	257/E21.668; 257/E21.703;		Noble, Wendell P.						US
11			US 6046477 A	20000404	9	Dense SOI programmable logic array structure	257/347	257/353; 257/304;		Noble, Wendell P.						US

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